IN THE CLAIMS

1. (Withdrawn) A method of manufacturing input and output terminal of a semiconductor device including an enhancement transistor having a channel region and an open drain transistor having a channel region , wherein the method of manufacturing the enhancement transistor comprises the steps of :

forming a gate insulating layer in an active region on a first conductive-type semiconductor substrate,

forming an impurity implantation region at a predetermined portion within the substrate of the lower side of the gate insulating layer through ion implantation of a second conductive-type impurity of low concentration,

forming a gate on the gate insulating layer by forming conductive layer on the whole surface of the resulting product and selectively-etching it so that a predetermined portion of the impurity implantation region and a predetermined portion of the substrate surface being close to the region being connected to the predetermined portion of the impurity implantation region are included at a predetermined portion, and

forming source and drain regions within the substrate at both edges of the gate through ion-implantation process of second conductive type of high concentration impurity.

2. (Withdrawn) The method of manufacturing input and output terminal of a semiconductor device as defined in claim 1, wherein the gate has a deposition layer such as "W-silicide/polysilicon", or a single layer of polysilicon.

3. (Withdrawn) A method of manufacturing input and output terminal of a semiconductor device including an enhancement transistor having a channel region and an open drain transistor having a channel region, wherein the method of manufacturing the enhancement transistor comprises the steps of :

forming a gate insulating layer in an active region on a first conductive-type semiconductor substrate,

forming an impurity implantation region at a predetermined portion within the substrate of the lower side of the gate insulating layer through ion implantation of a second conductive-type impurity of low concentration,

forming a gate on the gate insulating layer by forming conductive layer on the whole surface of the product and selectively-etching it so that the impurity implantation region and the substrate surface therearound are included at a predetermined portion, and

forming source and drain regions within the substrate at both edges of the gate through ion-implantation process of second conductive type of high concentration impurity.

4. (Withdrawn) The method of manufacturing input and output terminal of a semiconductor device as defined claim 3, wherein the gate has a deposition layer such as "W-silicide/polysilicon", or a single layer of polysilicon.

5. (Currently amended) A pull-up transistor disposed between a Vdd terminal and an I/O pad of a semiconductor device comprising:

a semiconductor substrate of a first conductivity type;

a source region and a drain region of a second conductivity type formed in the substrate and defining between them a channel region, one of the source region and the drain region being electrically coupled to the I/O pad, the other one of the source region and the drain region being electrically coupled to the Vdd terminal;

an impurity implantation region of impurities of a second conductivity type formed in ~~a first sector of~~ the channel region, the ~~first sector~~ impurity implantation region separated from the source region and the drain region; the impurity implantation region comprising a depletion channel of the second conductivity ~~type completely~~ type, the impurity implantation region ~~occupying~~ including a first surface ~~region~~ of the semiconductor substrate, wherein a ~~lateral extent~~ line width of the first surface ~~region~~ is equal to a ~~lateral extent~~ line width of the impurity implantation region;

~~a second sector of the channel region exclusive of the first sector comprising~~ an enhancement channel of the first conductivity type with uniform doping concentration and occupying a second surface ~~region~~ of the semiconductor substrate;

a gate insulating layer on the substrate over at least a portion of the first surface ~~region~~ and the second surface ~~region~~; and

a gate on the gate insulating layer over at least a portion of the ~~first sector~~ depletion channel and over at least a portion of the ~~second sector~~ enhancement channel, wherein the gate has a narrowest width that is greater than a line width of the impurity implantation region.

6. (Currently amended) The transistor of claim 5, wherein the ~~first sector~~ the impurity implantation region has a narrower line width than a line width of the gate.

7. (Currently amended) The transistor of claim 5, in which

the gate comprises a first portion over the ~~first sector~~ enhancement channel and a second portion over the ~~second sector~~ depletion channel; and

the first portion is in a predetermined ratio with respect to the second portion.

8. (Cancelled)

9. (Currently amended) The transistor of claim 5, wherein the ~~first sector~~ impurity implantation region is separated from the source region and from the drain region by substantially equal distances.

10. (Currently amended) A pull-up transistor disposed between a Vdd terminal and an I/O pad of a semiconductor device comprising:

a semiconductor substrate of a first conductivity type;

a source region and a drain region of a second conductivity type formed in the substrate and defining between them a channel region, one of the source region and the drain region being electrically coupled to the I/O pad, the other one of the source region and the drain region being electrically coupled to the Vdd terminal;

a first sector of the channel region, the first sector not reaching either one of the source region and the drain region;

an impurity implantation region formed on the semiconductor substrate, having impurities of a second conductivity type, and with a lateral extent coextensive with the first sector, the impurity implantation region further comprising a first surface region that functions as a depletion channel and that occupies the entire top surface of the semiconductor substrate within the lateral extent of the impurity implantation region;

a second sector of the channel region exclusive of the first sector, the second sector comprising a second surface region that functions as an enhancement channel, that occupies an entire surface of the semiconductor substrate in the second sector, and that has uniform doping concentration of the first conductivity type;

a gate insulating layer on the substrate over at least a portion of the first surface region and the second surface region; and

a gate on the gate insulating layer over at least a portion of the first sector and over at least a portion of the second sector, wherein the gate has a narrowest width that is greater than the lateral extent of the impurity implantation region.

11. (Original) The transistor of claim 10, wherein the first sector has a narrower line width than a line width of the gate.

12. (Previously presented) The transistor of claim 10, in which

the gate comprises a first portion over the first sector and a second portion over the second sector; and

the first portion is in a predetermined ratio with respect to the second portion.

13. (Previously presented) The transistor of claim 10, wherein the first sector is separated from the source region and from the drain region by substantially equal distances.

14. (Currently amended) A pull-up transistor disposed between a Vdd terminal and an I/O pad of a semiconductor device comprising:

a semiconductor substrate of a first conductivity type;

a source region and a drain region of a second conductivity type formed in the substrate and defining between them a channel region, one of the source region and the drain region being electrically coupled to the I/O pad, the other one of the source region and the drain region being electrically coupled to the Vdd terminal;

a first sector of the channel region, the first sector not reaching either one of the source region and the drain region;

an impurity implantation region formed on the semiconductor substrate, having impurities of a second conductivity type, and with a lateral extent coextensive with the first sector, the impurity implantation region further comprising a first surface region that functions as a depletion channel and that occupies the entire top surface of the semiconductor substrate within the first sector~~, the impurity implantation region having a top surface and a bottom surface, wherein the top surface is larger than the bottom surface~~;

a second sector of the channel region exclusive of the first sector, the second sector comprising a second surface region that functions as an enhancement channel, that occupies an entire surface of the semiconductor substrate in the second sector, and that has uniform doping concentration of the first conductivity type;

a gate insulating layer on the substrate over at least a portion of the first surface region and the second surface region; and

a gate on the gate insulating layer over at least a portion of the first sector and over at least a portion of the second sector, wherein the gate has a narrowest width that is greater than the lateral extent of the impurity implantation region.

15. (Previously presented) The transistor of claim 14, wherein the first sector has a narrower line width than a line width of the gate.

16. (Previously presented) The transistor of claim 14, in which

the gate comprises a first portion over the first sector and a second portion over the second sector; and

the first portion is in a predetermined ratio with respect to the second portion.

17. (Previously presented) The transistor of claim 14, wherein the first sector is separated from the source region and from the drain region by substantially equal distances.

18. (New) An input and output terminal structure of a semiconductor device, comprising:

a Vdd terminal;

an I/O pad;

an open drain transistor with a source region and a drain region defining between them a channel region, and a gate having a length, one of the source region and the drain region being electrically coupled to the Vdd terminal, the other one of the source region and the drain region being grounded; and

an enhancement transistor with a gate having a length that is greater than a length of the gate of the open drain transistor and with a source region and a drain region defining between them a channel region, one of the source region and the drain region being electrically coupled to the I/O pad, the other one of the source region and the drain region being electrically coupled to the Vdd terminal.

19. (New) The structure of claim 18, wherein the enhancement transistor comprises:

a semiconductor substrate of a first conductivity type, wherein the source region and the drain region are of a second conductivity type and formed in the semiconductor substrate;

an impurity implantation region having impurities of the second conductivity type that is formed in the channel region, that is separated from the source region and the drain region, and that includes a first surface of the semiconductor substrate, the impurity implantation region configured to function as a depletion channel;

an enhancement channel of the first conductivity type with uniform doping concentration, the enhancement channel including a second surface of the semiconductor substrate; and

a gate insulating layer on the semiconductor substrate over at least a portion of the first surface and the second surface.

20. (New) The structure of claim 18, wherein the length of the gate of the open drain transistor is equal to a length of an impurity implantation region formed in a channel region of the open drain transistor.

21. (New) The structure of claim 18, wherein the length of the gate of the enhancement transistor is greater than a length of an impurity implantation region formed in a channel region of the enhancement transistor.

22. (New) The structure of claim 18, wherein one of the source region and the drain region of the open drain transistor is electrically coupled to one of the source region and the drain region of the enhancement transistor, and the other one of the source region and the drain region of the open drain transistor is grounded.

23. (New) The structure of claim 18, wherein one of the source region and the drain region of the enhancement transistor is electrically coupled to one of the source region and the drain region of the open drain transistor, and the other one of the source region and the drain region of the enhancement transistor is electrically coupled to the Vdd terminal.

24. (New) The structure of claim 18, wherein the impurity implantation region is separated from the source region by a predetermined distance.

25. (New) The structure of claim 18, wherein the impurity implantation region is separated from the drain region by a predetermined distance.

26. (New) The structure of claim 18, wherein the impurity implantation region is separated from the source region and the drain region by substantially equal distances.